CLAIMS

What is claimed is:

1. An integrated circuit package comprising:

a substrate having a first surface and a second surface;

a first die pad area, disposed on said first surface, said die pad area having dimensions suitable to mount an integrated circuit thereon;

a plurality of thermally conductive signal elements disposed on the first surface of the substrate outside the die pad area, comprising a first signal pad row and at least one additional signal pad row; and

a first plurality of thermally conductive thermal fingers extending from said die pad area and thermally coupled thereto, said thermal fingers encompassing at least some individual ones of the pads of the first signal pad row.

2. An integrated circuit package as in claim 1, further comprising on said second surface,

a second die pad, disposed on said second surface, said second die pad area underlying said first die pad area;

a second plurality of thermally conductive signal elements disposed on the second surface of the substrate outside the second die pad area , comprising a first signal pad row and at least one additional signal pad row; and

a second plurality of thermally conductive thermal fingers on said second surface extending from said second die pad area on the second surface and thermally coupled thereto, said thermal fingers encompassing at least some individual ones of the pads of the first signal pad row on said second surface.

3. An integrated circuit package as in claim 1, further comprising:

a plurality of vias, one or more of the vias coupled to an associated signal element, the one or more vias providing at least thermal conductivity from the first surface of the substrate to the second surface of the substrate.

4. An integrated circuit package as in claim 1, wherein said second surface comprises a substantially continuous layer of thermally conductive material underlying said first die pad area and said first plurality of thermally conductive thermal fingers.

5. An integrated circuit package as in claim 2, wherein the thermal fingers of the second surface are in registration with and underlie the thermal fingers on the first surface:

6. An integrated circuit package as in claim 2, wherein the thermal fingers of the second surface are offset from the thermal fingers on the first surface.

7. An integrated circuit package of claim 2, wherein the substrate is thermally coupled to a printed wiring board and the thermal energy is dissipated from the die pad area of the first surface to the die pad area of the second surface to the printed wiring board through said first and second thermal fingers.

8. An integrated circuit package as in claim 1, further comprising an integrated circuit disposed on the die pad area.

9. An integrated circuit package as in claim 1, wherein the thermal fingers are thermally coupled to a plurality of electrical signal conveying vias disposed between said first and second surfaces.

10. An integrated circuit package comprising:

a substrate having a first surface and a second surface;

a first die pad area, disposed on said first surface, said die pad area having dimensions suitable to mount an integrated circuit thereon;

a plurality of thermally conductive signal elements disposed on the first surface of the substrate surrounding the die pad area, comprising a first signal pad row and at least one additional signal pad row;

where an outer edge of said die pad area is formed to comprise a plurality of relief structures, where at least some individual ones of said relief structures at least partially surround at least one of said signal pads of said first signal pad row.

11. An integrated circuit package as in claim 10, further comprising on said second surface,

a second die pad, disposed on said second surface, said second die pad area underlying said first die pad area;

a second plurality of thermally conductive signal elements disposed on the second surface of the substrate surrounding the die pad area, comprising a first signal pad row and at least one additional signal pad row;

where an outer edge of said second die pad area is formed to comprise a plurality of relief structures, where at least some individual ones of said relief structures at least partially surround at least one of said signal pads of said first signal pad row on said second surface.

12. An integrated circuit package as in claim 10, wherein said second surface comprises a substantially continuous layer of thermally conductive material underlying said first die pad area and said first plurality of relief structures.

13. A method for dissipating thermal energy from a die pad comprising:

providing a substrate having a first surface and a second surface and a first thermally conductive die pad disposed on said first surface, said die pad comprising a first plurality of relief structures formed on an outer edge, where at least some individual ones of said relief structures at least partially surround at least one signal pad of a first signal pad row on said first surface and are thermally coupled thereto; and

conveying thermal energy using a plurality of thermally conductive vias coupled to said signal pads, for providing thermal conductivity from the first surface of the substrate to the second surface of the substrate.

14. A method as in claim 13, further comprising:

providing a second thermally conductive die pad disposed on said second surface, underlying said first die pad on said first surface, said die pad comprising a second plurality of relief structures formed on an outer edge, where at least some individual ones of said relief structures at least partially surround at least one second signal pad of a first signal pad row on said second surface and are thermally coupled thereto; and

transferring thermal energy from the first surface to the second surface and to a printed wiring board.

15. A method as in claim 13, wherein said second surface comprises a substantially continuous layer of thermally conductive material underlying said first die pad and said first plurality of thermally conductive relief structures.

16. A method as in claim 14, wherein selected vias are located under the die pad for conducting thermal energy from the first die pad to the second die pad to the printed wiring board.

17. A method as in claim 13, further comprising mounting an integrated circuit on the die pad.

18. A method as in claim 13, further comprising:

electrically isolating the plurality of thermally conductive relief structures from signal pads on the substrate.